

Amendments to the Claims

1. **(Currently Amended)** A signal processor for subjecting data read from a recording medium to predetermined digital signal processing, and subjecting the data, which has been subjected to the predetermined digital signal processing, to error correction for each predetermined error correction block, said signal processor comprising:

B² a first memory operable to ~~means for~~ sequentially ~~store~~ storing the data which has been subjected to the predetermined digital signal processing;

an error correction block operable to ~~subject~~ ~~means for subjecting~~ the data, which has been stored in said first memory ~~subjected to the predetermined digital signal processing~~, to error correction for each predetermined error correction block;

a second memory;

a descrambling/error detection block operable to read the data after the error correction from said first memory, ~~means for descrambling~~ ~~descramble~~ the data which has been subjected to the error correction, ~~and detecting~~ ~~detect~~ errors in the data after the descrambling, and thereafter store the data in said second memory; and

a controller operable to transmit ~~control~~ ~~means for transmitting~~ error-free data which has been stored in said second memory to a host computer when said descrambling/error detection block judges that there is no error in the data which has been stored in said second memory subjected to the error detection.

2. **(Currently Amended)** A signal processor as described in Claim 1, wherein said error correction block ~~means~~ comprises:

a syndrome calculator operable to calculate ~~for calculating~~ syndrome of the data which has been subjected to the predetermined digital signal processing;

an error position/pattern calculator operable to calculate ~~an~~ ~~for calculating the~~ error position and ~~an~~ the error pattern after the syndrome calculation;

an error correction result holding block operable to hold ~~means for holding~~ information as to whether or not the data detected by said ~~the~~ error position/pattern calculator is error-correctable ~~or not~~;

a data correction block operable to read erroneous data stored in said first memory, means for correcting correct errors in the data, and store the data which has been subjected to the error correction in said first memory based on the basis of the result of the syndrome calculation the error position and the error pattern calculated by said error position/pattern calculator; and

a number-of-error-correction control block operable to ~~means for controlling the control a~~ number of error corrections.

B2 3. **(Currently Amended)** A signal processor as described in Claim 1, wherein said descrambling/error detection block means comprises:

a first memory interface operable to read the data stored in said first memory;

a descrambling block operable to ~~means for descrambling~~ descramble the data after the error correction which has been read from said first memory ~~corrected by the error correction means~~;

an error detection block operable to detect ~~means for detecting~~ errors in the descrambled data; and

a second memory interface operable to store the descrambled data in said second memory; and

an error detection result holding block operable to hold a ~~means for holding the~~ result of the error detection as to whether there is any error in the data which has been subjected to the error detection.

4. **(Currently Amended)** A signal processor as described in Claim 1, wherein:

the data which has been stored in said second memory ~~subjected to the predetermined digital signal processing~~ is read ~~from the memory means~~ for each predetermined error correction block, followed by error detection and error correction when said descrambling/error detection block judges that there is no error in the data stored in said second memory;

when there is some error, the error is corrected by said ~~the~~ error correction ~~means~~ block for each predetermined error correction block; and

B2 when there is no error, the data is transmitted to the host computer for each predetermined error correction block.
